WHAT IS CLAIMED IS:

1. A memory comprising:

an array of volatile memory cells;

addressing circuitry for providing access to selected ones of said memory cells;

master read/write circuitry for reading and writing data into said selected ones of said cells;

first slave circuitry for storing data for exchange with said master read/write circuitry;

second slave circuitry for storing data for exchange with said master read/write circuitry; and

control circuitry for controlling exchange of data between said master read/write circuitry and said first and second slave circuitry.

2. The memory of Claim 1, wherein said control circuitry is further operable to control the exchange of data between said master read/write circuitry and said first slave circuitry during a first access cycle and between said master read/write circuitry and said second slave circuitry during a second subsequent access cycle.

3. The memory of Claim 1 wherein said array comprises an array of dynamic random access memory cells.

4. The memory of Claim 1 wherein said addressing circuitry comprises a row decoder for selecting a row of cells in said array.

5. The memory of Claim 1 wherein said master read/write circuitry comprises a plurality of sense amplifiers.

6. The memory of Claim 1 wherein each of said first and second slave read/write circuitry comprises a plurality of sense amplifiers.

7. A memory system comprising:

an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline;

a row decoder coupled to said wordlines;

a bank of master sense amplifiers coupled to said bitlines;

a plurality of banks of slave sense amplifiers coupled to said master sense amplifiers;

a column decoder coupled to each of the plurality of slave sense amplifiers; and

control circuitry coupled to said row decoder, said bank of master sense amplifiers and said banks of slave sense amplifiers.

8. The memory system of Claim 7 wherein said control circuitry comprises:

mode control circuitry coupled to said row decoder and said master sense amplifiers; and

multiplexer control circuitry coupled to said mode control circuitry and said first and second banks of slave sense amplifiers.

~~8.~~ 9. The memory system of Claim 7 wherein said control circuitry is operable during a read operation to:

control ~~the~~ sensing by said master sense amplifiers of first data from first said row in said array selected by said row decoder;

control ~~the~~ transfer of said first data from said master sense amplifiers to a first one of said banks of slave sense amplifiers;

control ~~the~~ sensing by said master sense amplifiers of second data from a second said row in said array selected by said row decoder; and

control ~~the~~ transfer of said second data from said master sense amplifiers to a second one of said banks of slave sense amplifiers.

9 10. The memory system of Claim 8 wherein said column decoder is operable during a read operation in response to at least one column address to:

output selected ones of said first data presented by said first one of said banks of slave amplifiers; and

following the output of said first data, output selected ones of said second data presented by said second one of said banks of slave amplifiers.

10 11. The memory system of Claim 7 wherein said control circuitry is operable during a write operation to:

control ~~the~~ transfer of first data from said column decoder to a first one of said banks of slave sense amplifiers;

control ~~the~~ writing of said first data into first selected ones of said cells in said array through said master sense amplifiers;

control ~~the~~ transfer of second data from said column decoder to a second one of said banks of slave sense amplifiers; and

control ~~the~~ writing of said second data into second selected ones of said cells in said array through said master sense amplifiers.

11 12. The memory system of Claim 10 wherein said control circuitry is operable during said write operation to transfer said second data from said column decoder to said second one of said banks of slave sense amplifiers

concurrently with the writing of said first data into said array.

13. The memory system of Claim 8 wherein said control circuitry is operable during a move operation to:

control the sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

control the transfer of said data from said master sense amplifiers to a selected one of said banks of slave sense amplifiers;

control the writing of said data through said master sense amplifiers to a second said row in said array selected by said row decoder.

14. The memory system of Claim 8 wherein said control circuitry is operable during a block move operation to:

control the sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

control the transfer of said data from said master sense amplifiers to a selected one of said banks of slave amplifiers;

control the shifting of said data from a first set of sense amplifiers to a second set of sense amplifiers within said selected bank of slave amplifiers; and

control the writing of said data through said master sense amplifiers to ones of said cells along said selected said row associated with said bitlines coupled to said second set of sense amplifiers.

15. A memory comprising:

an array of dynamic random access memory cells arranged in rows and columns, each said row including a conductive wordline and each said column including a conductive bitline;

row decoder circuitry coupled to said wordlines for selecting a said row in response to a row address;

sense amplifier circuitry coupled to said bitlines for reading and writing data to ones of said cells along a selected said row;

column decoder circuitry coupled to a data bus;

first latching circuitry coupled to said sense amplifier circuitry by a first local bus and to said column decoder by a second local bus for latching data being exchanged between said sense amplifier circuitry and said column decoder;

second latching circuitry coupled to said sense amplifier circuitry by said first local bus and to said column decoder by said second local bus for latching data being exchanged between said sense amplifier circuitry and said column decoder; and

control circuitry for controlling said first and second latching circuitry, said control circuitry alternately latching data being exchanged between said sense amplifier circuitry and said column decoder in said first latching circuitry and said second latching circuitry.

16. The memory of Claim 15 wherein said first and second latching circuitry comprise sense amplifier circuitry.

17. The memory of Claim 15 and further comprising input/output control circuitry coupled to said row decoder and said column decoder by an address bus, said

input/output control circuitry operable to present row and column addresses received from an external source on said address bus for selecting ones of said rows and columns.

16. The memory of Claim 15 wherein said input/output control circuitry is further operable to internally generate row addresses for presentation on said address bus.

19. A method for reading data from a memory including an array of memory cells arranged in rows and columns each said row associated with a conductive wordline and each said column associated with a conductive bitline, comprising the steps of:

selecting a first row to be read by activating the associated wordline;

sensing the bitlines with a bank of master sense amplifiers to read data stored in the cells of the first row;

latching the data read from the cells of the first row in a first set of slave sense amplifiers;

selecting a second row to be read by activating the associated wordline;

sensing the bitlines with the master sense amplifiers to read data stored in the cells of the second row; and

latching the data read from the cells of the second row in a second set of slave sense amplifiers.

20. The method of Claim 19 and further comprising the step of outputting selected ones of the data from said first row substantially simultaneous with said steps of selecting and sensing the data from the second row.

21. A method for writing data to a memory including an array of memory cells arranged in rows and columns each said row associated with a conductive wordline and each said column associated with a conductive bitline, comprising the steps of:

latching first data in a first bank of slave sense amplifiers;

writing the first data into first selected cells in said array;

substantially concurrently with said step of writing the first data, latching second data in a second bank of slave sense amplifiers; and

writing the second data into second selected cells in the array upon the completion of said step of writing the first data.

22. A method of performing a block transfer within a memory including an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline, comprising the steps of:

selecting a row in the array;

sensing the bitlines of the array to read data stored in the cells of the selected row with a bank of master sense amplifiers;

latching the data read from the cells of the selected row in a bank of slave sense amplifiers;

writing data through the master sense amplifiers to other cells in the array.

23. The method of Claim 22 wherein said step of writing comprises the step of writing data to other cells in the selected row in the array.

24. The method of Claim 22 wherein said step of writing comprises the step of writing data to cells of another row in the array.